

ADS1244EVM ADS1245EVM

Evaluation Module

User's Guide

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During normal operation, some circuit components may have case temperatures greater than 60°C. The EVM is designed to operate properly with certain components above 60°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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Preface

Read This First

About This Manual

This manual describes the ADS1224EVM and ADS1245EVM evaluation fixtures and how to use them.

Notational Conventions

The ADS1244EVM and ADS1245EVM boards are identical except for the evaluation device installed on them. This manual covers both boards, and refers to them in the singular, when necessary, as “ADS1244/45EVM.”

When a statement applies to both the ADS1244 and ADS1245 devices, they may be referred to in the singular, when necessary, as “ADS1244/45.”

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This is an example of a caution statement.

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Data sheets	Literature number
ADS1244	SBAS273
ADS1245	See http://www.ti.com/
REF1004	SBVS002
SN74LVC1G80	SCES221

FCC Warning

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Introduction

The ADS1244EVM and ADS1245EVM are evaluation fixtures for the ADS1244 and ADS1245 24-bit delta-sigma analog-to-digital converters. Designed for prototyping and evaluation, they include a reference circuit and an oscillator circuit with two selectable frequencies.

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1.1 Introduction

Many data converter evaluation fixtures contain a computer interface or a microcontroller, but the ADS1244/45EVM contains only the ADS1244 or ADS1245 device and a few support components. All ADS1244/45 pins are accessible through various pins on the ADS1244/45EVM's analog and digital connectors.

The ADS1244/45EVM is designed using a simple card format developed by TI. This simple, consistent design makes it very easy to connect the ADS1244/45EVM to your own prototype system. You can even think of the ADS1244/45EVM as an alternate package for the ADS1244/45 – one much larger than the device itself, but also much easier to wire up by hand on your test bench.

The ADS1244/45EVM can be plugged directly into suitable motherboards such as the HPA449 MSP430 microcontroller development system from Soft-Baugh, Inc. (<http://www.softbaugh.com/>). See TI's web site for sample code using the ADS1244/45EVM with the HPA449.

The ADS1244/45EVM, together with the HPA449 and the appropriate software, also forms a complete evaluation system for verifying the performance of the ADS1244/45. See TI's web site for more information and software.

1.2 Built-in Accessories

The ADS1244/45EVM includes a system clock generator and a low-noise voltage reference. Both features are optional; you can select an external system clock and an external reference using the slide switches.

The +2.5V reference circuit is based on a REF1004–2.5. Its noise performance is sufficient to allow the ADS1244/45 to perform at its lowest noise level.

The system clock is based on a 4.9152MHz CMOS crystal clock generator module. A flip-flop divides the clock generator by two in order to provide an additional 2.4576MHz clock source. The two clocks can be selected using the clock source select switch.

1.3 Connectors

The ADS1244/45 device on the ADS1244/45EVM is connected through three headers: the analog connector, the serial connector, and the power connector. Pinouts and locations for the connectors are given in the following chapter.

The **analog connector** (J1) carries analog I/O. The ADS1244/45 has a single differential input channel connected to pins 1 and 2. An optional external differential reference can be connected to pins 18 and 20.

The **serial connector** (J5) carries the ADS1244/45 serial digital interface, an optional external system clock signal, and an I²C connection to the on-board serial EEPROM.

The **power connector** (J6) carries the power supplies. The ADS1244/45EVM requires a +5V analog supply and either a +5V or +3.3V digital supply. The board is designed using a single ground net connected to DGND. An AGND pin is also provided, and it can be connected to DGND using jumper J2.

The ADS1244/45 uses separate supplies for its analog and digital sections. A jumper is inserted in each supply line. These jumpers allow the current of each supply to be measured independently.

Four loop-style testpoints provide easy access to the ADS1244/45 clock and the power supplies on the board. Other signals can be probed using the I/O connector pins.

1.4 Controls

The ADS1244/45EVM is configured using four slide switches and a jumper.

Switch S1 selects the system clock source for the ADS1244. You can select from the 4.9152MHz clock source, the 2.4576MHz clock source, or an externally provided clock. When the external clock is selected, the onboard oscillator is disabled to save power and prevent interference.

Switch S2 selects the input signal provided to the ADS1244/45. Normally you will use the external input, but you can also use the switch to short the inputs together and to connect the reference voltage to the inputs. The latter two positions are useful for conducting noise tests.

Switch S3 selects the reference input. One position selects the external reference input pins on the analog connector (J1). The other two positions connect the onboard +2.5V reference in one of two ways: between ground and the reference, or between the reference and the analog supply.

Switch S5 is used to select one of two digital power supply pins provided on the power connector. One pin is used for +3.3V, and the other is used for +5V; some motherboards, such as the HPA449, provide both voltages. This switch determines the logic levels that the ADS1244/45 will use to communicate, so it is important to set it correctly.

1.5 Setting Up

The way you configure the ADS1244/45EVM depends on how you will use it. There is therefore no single correct procedure to follow to configure the ADS1244/45EVM.

Nevertheless, it is useful to remember the following things when you are setting up the board:

- ☐ Make certain that S5, the digital power supply select switch, is in the right position for your system, and that you have a power supply connected to the proper pins on the power connector.
- ☐ If you are not measuring the ADS1244/45's supply current, remember to place shorting blocks on jumpers J3 and J4. Without these blocks, the ADS1244/45 will not be powered on, and will not work properly, if at all.
- ☐ Unless you are using two entirely separate power supplies for analog and digital, place a shorting block on jumper J2. This connects the analog and digital grounds together, which is the usual way to operate the ADS1244/45.
- ☐ Check the system clock switch. If it is set to "EXT," and you have not connected a clock signal to the external clock input pin on J5, the ADS1244/45 will not operate.



Circuit Description

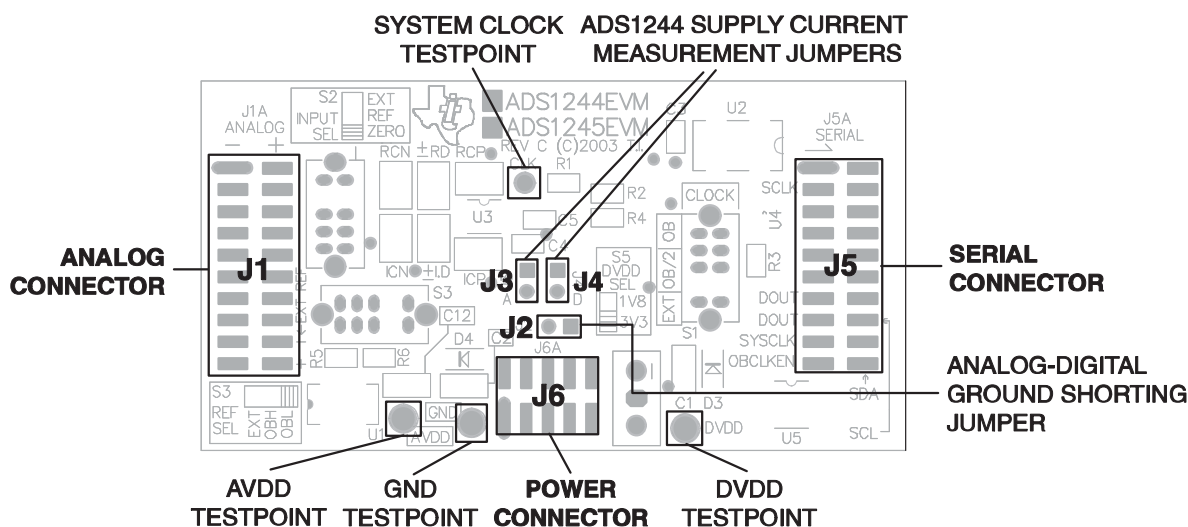
This chapter describes the ADS1244/45EVM connectors, controls, and circuit design in detail.

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2.1 I/O Connectors and Testpoints

The positions and functions of the connectors and testpoints are shown in Figure 2-1.

Figure 2-1. Connectors and Jumpers



Many of the pins on the connectors are not used. On the pinout diagrams, unused pins are not marked. In the pin description tables, unused pins are not listed, and ground pins are listed together, with the exception of the power connector.

J1, J5, and J6, though treated as a single connector, are actually mounted as connector pairs in a pass-through configuration. Each pair has a male surface-mount header on the top (component) side of the board, and a corresponding female surface-mount socket on the bottom (solder) side of the board. The headers, mounted on top, are suffixed A, and the sockets, mounted on bottom, are suffixed B.

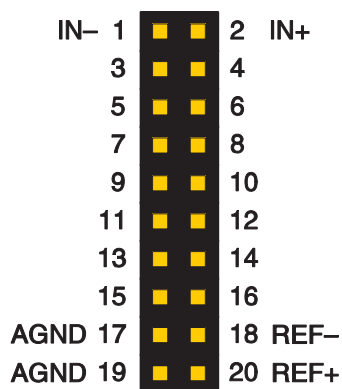
In the schematic, the connector pairs are shown as one symbol. For J1, J5, and J6, all bottom-side pins are connected to their corresponding top-side pins; for example, J1B pin 1 connects to J1A pin 1, J1B pin 2 connects to J1A pin 2, etc. This scheme is used with every pin on connectors J1, J5, and J6.

In the following descriptions, we will treat the connector pairs as a single connector.

2.1.1 J1: Analog Connector

The analog connector pinout is shown in Figure 2–2. and described in Table 2–1.

Figure 2–2. Analog Connector Pinout



Caution: Although certain pins are described as “negative,” *never* apply voltages less than -0.3V to these pins. The ADS1244 is not a bipolar-input device, and it cannot accept negative voltages below -0.3V without damage. The negative input pins are so named because the voltage on such a pin is subtracted from a positive pin during a reading.

Table 2–1. Analog Connector Pin Descriptions

Pin No.	Pin Name	Standard Name	Direction	Function
1	SYSINN	AN0-	Input	Negative analog input
2	SYSINP	AN0+	Input	Positive analog input
18	SYSREFN	REF-	Input	Negative external reference input
20	SYSREFP	REF+	Input	Positive external reference input
17, 19	GND	AGND	Power	Signal ground

Note that the input pins are not used unless the input select switches are set to the appropriate positions. See Table 2–3 for details.

2.1.2 J5: Serial Connector

The serial connector's pinout is shown in Figure 2–3 and described in Table 2–2.

Figure 2–3. Serial Connector Pinout

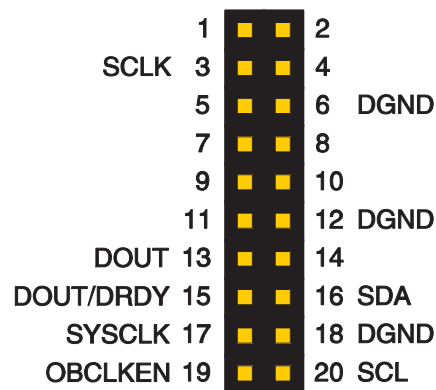


Table 2–2. Serial Connector Pin Descriptions

Pin No.	Pin Name	Standard Name	Direction	Function
3	SCLK	CLKX	Input	Serial clock input
13	DOUT	DR	Output	Serial data output / data ready
15	DOUT	INT	Output	Serial data output / data ready
16	SCL	SCL	I/O	I ² C clock line
17	SYSCLK	TOUT	Input	External system clock input
19	OBCLKEN	GPIO5	Output	Clock mode indicator
20	SDA	SDA	I/O	I ² C data line
6, 12, 18	GND	DGND	Power	Signal ground

The ADS1244/45 serial interface is connected through pins 3, 13, and 15.

SCL and SDA are used to communicate with the I²C serial EEPROM.

OBCLKEN is logic high when either of the onboard clock sources are selected, and low when the external clock source is selected. It can be used by external systems to determine whether to generate a clock signal for the ADS1244/45EVM.

2.1.3 J6: Power Connector

The power connector pinout pattern is shown in Figure 2–4 and described in Table 2–3.

Figure 2–4. Power Connector Pinout

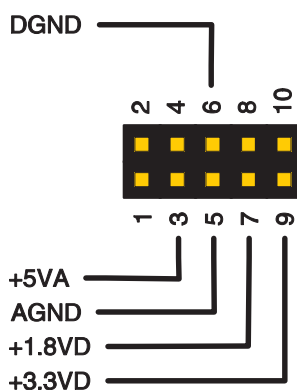


Table 2–3. Power Connector Pin Descriptions

Pin No.	Pin Name	Function	Usage on ADS1244/45EVM
1	+VA	Positive analog supply, +5V to +18V	Not used
2	–VA	Negative analog supply, –5V to –18V	Not used
3	+5VA	Positive analog supply, +5VA	Analog supply
4	–5VA	Negative analog supply, –5VA	Not used
5	AGND	Analog ground	Optionally connected to DGND through J2
6	DGND	Digital ground	Ground
7	+1.8VD	Positive digital supply, +1.8V	Possible digital supply, selected using S5
8	VD1	Positive digital supply	Not used
9	+3.3VD	Positive digital supply, +3.3V	Possible digital supply, selected using S5
10	+5VD	Positive digital supply, +5V	Not used

The ADS1244/45EVM always uses DGND for its single ground domain. The AGND pin may optionally be connected to DGND through jumper J2.

The ADS1244/45 uses an analog supply of +5V and a digital supply of +1.8V to +3.3V. Both +1.8V and +3.3V are available as standard supply voltages over the power connector, so the ADS1244/45EVM allows you to switch between them using S5.

2.1.4 Testpoints

The testpoints are marked on the board with the net to which they are attached, instead of with their schematic reference designators. Table 2–4 lists the testpoints.

Table 2–4. Testpoints

Board Marking	Reference Designator	Signal
CLK	TP4	System clock
AVDD	TP3	Analog supply
DVDD	TP1	Digital supply
GND	TP2	Ground

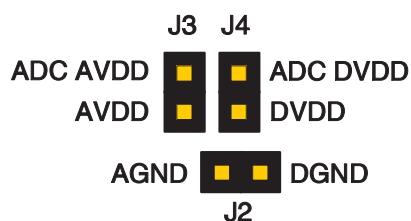
The CLK testpoint is attached to the CLK pin on the ADS1244/45. It reflects the actual CLK signal controlling the ADS1244/45. When the onboard oscillator is in use, its waveform can be observed from the CLK testpoint.

The supply testpoints are provided for convenience. The GND testpoint is slightly larger than the others to accommodate multiple probe clips.

2.2 Jumpers

The jumpers are shown in Figure 2–5. Jumper positions and functions are shown in Figure 2–1.

Figure 2–5. Jumpers



2.2.1 J2: Analog–Digital Ground Shorting Jumper

This jumper is used to connect the analog and digital grounds together.

If you are using a single power supply, you should usually place a shorting block across this jumper. If you are using two different supplies, each with its own ground, you should usually leave this jumper unconnected.

2.2.2 J3: ADS1244/45 Analog Supply Current Measurement Jumper

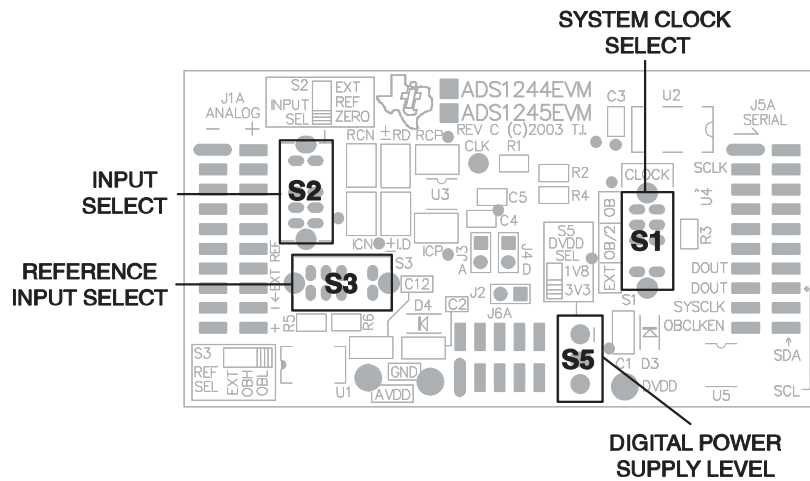
This jumper can be used to measure the current drawn by the ADS1244/45 analog supply line.

For normal operation, when not measuring current, place a shorting block across this jumper.

2.3 Switches

The positions and functions of the switches are shown in Figure 2–6.

Figure 2–6. Switches



2.3.1 S1: System Clock Select

This switch selects which of the three available clock sources on the ADS1244/45EVM will be provided to the CLK pin on the device. The switch positions are described in Table 2–5.

Table 2–5. System Clock Select Switch

Board Marking	Switch Position	System Clock Source	OBCLKEN State
OB	Top	Onboard 4.9152MHz	High
OB/2	Middle	Onboard 2.4576MHz	High
EXT	Bottom	External (J5, pin 17)	Low

This switch also controls the state of OBCLKEN. This signal enables the oscillator (U2), and is also brought to pin 19 of J5. External systems can read this signal to determine whether to generate a clock.

2.3.2 S2: Input Select

This switch controls which lines are routed to the ADS1244/45 input pins. The switch positions are described in Table 2–6.

Table 2–6. Input Select Switch

Board Marking	Switch Position	Input Source	ADS1244/45 VIN+	ADS1244/45 VIN–
EXT	Top	External (J1, pins 1 and 2)	J1 pin 2	J1 pin 1
REF	Middle	Reference voltage	+2.5V	Ground
ZERO	Bottom	Zero (shorted to reference)	+2.5V	+2.5V

In the EXT position, J1 pins 1 and 2 are connected to the ADS1244/45 inputs.

In the REF position, the reference is connected across the ADS1244/45 inputs. This normally gives a full-scale reading.

In the ZERO position, both of the ADS1244/45 input pins are connected to the reference. This gives a zero-scale reading.

The REF and ZERO positions are useful for certain noise tests.

2.3.3 S3: Reference Input Select

This switch controls which signals are connected to the ADS1244/45 differential reference input. The switch positions are described in Table 2–7.

Table 2–7. Reference Input Select Switch

Board Marking	Switch Position	Reference Source	ADS1244/45 REF+	ADS1244/45 REF–
EXT	Left	External (J1, pins 18 and 20)	J1 pin 20	J1 pin 18
OBH	Middle	On-board, high common-mode	+AVDD	+2.5V
OBL	Right	Zero (shorted to reference)	+2.5V	AGND

In the EXT position, J1 pins 18 and 20 are connected to the ADS1244/45 reference input.

In the OBH position, the analog power supply is connected to the positive reference input, and the negative reference input is connected to the output of the onboard reference.

In the OBL position, the onboard reference output is connected to the ADS1244/45 positive reference input pin, and the negative reference input pin is grounded.

Both OBH and OBL provide a +2.5V reference to the ADS1244/45. The OBL position corresponds to the usual way to connect a reference to the ADS1244/45, and should be used for most measurements. The OBH position is useful for testing the reference input common-mode sensitivity, which can be important for ratiometric connections.

2.3.4 S5: Digital Power Supply Level

This switch selects from one of the two digital power supply pins on J6 that can be used to power the digital side of the ADS1244/45 device. The positions of the switch are described in Table 2–8.

Table 2–8. Digital Power Supply Level Select Switch

Board Marking	Switch Position	Digital Power Supply Source
1V8	Top	+1.8V typ. (J6 pin 7)
3V3	Bottom	+3.3V typ. (J6 pin 9)

This switch determines the logic level at which the ADS1244/45 will communicate. Make certain it is set correctly before you power the board on.

Usage

This chapter provides guidelines on using the ADS1244/45EVM and connecting other systems to it.

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3.1 The Input Filtering Capacitors

The ADS1244/45EVM is designed to accept input filtering capacitors on both the reference and signal inputs. Each input has two common-mode capacitors and one differential capacitor.

The common-mode capacitors are connected from each differential line to ground. They are intended to filter the common-mode portion of the signal. The differential capacitors are connected between the differential pins. These capacitors filter the signal itself.

The ADS1244/45EVM is shipped with a differential capacitor and common-mode capacitors on the analog inputs, and a positive common-mode capacitor on the reference. The other two reference filter capacitors are not populated, since they would be redundant with REF– connected to ground, as is usually the case.

The performance of the ADS1244 is often improved by these capacitors. On the input, the capacitors attenuate frequencies beyond the ADS1244/45 sampling frequency. On the reference, the capacitors eliminate high noise frequencies that can couple into the device and disrupt the measurement. (Lower noise frequencies can be dealt with at the reference circuit itself.)

Although the supplied 100nF capacitors do not have particularly high values, they are in relatively large 1210-size packages, in contrast to most of the other passives on the board. They were made large so that you can easily remove them or replace them with other values. By exercising appropriate care, you can even solder leaded devices to these large pads.

A typical layout will not use packages as large as this, unless very large capacitors are also used.

3.2 The Serial Interface

The ADS1244/45 serial interface is connected directly to the ADS1244/45EVM serial connector. Therefore, the way you connect the ADS1244/45EVM in a prototype situation can be the same as the way you connect it in your final product. This discussion assumes that you will be connecting the ADS1244/45EVM to a microcontroller, but for FPGA and PC-based systems, similar principles apply.

There are two primary ways to connect the ADS1244/45. If you are using GPIO (“bit-banging”) to communicate with the device, you can use only the serial data / data ready line (J5 pin 13) and the serial clock line (J5 pin 3). By polling the data line, you can determine when the ADS1244/45 has a new code ready. You might also let the data line interrupt the processor, if your processor supports this.

If the microcontroller has an SPI peripheral, you can also use this, together with an interrupt input, to read from the ADS1244/45. This is done by connecting the serial data line to both SDI / MOSI on the microcontroller and also to the interrupt input.

The ADS1244/45EVM is pre-wired for this method. The standard serial connector has an interrupt output pin (J5 pin 15). The data line is wired to both this pin and the serial data pin.

Of course, you can still use the bit-bang method to communicate with the ADS1244/45. Simply ignore the interrupt output pin and use GPIO instead of a dedicated SPI peripheral.

3.3 The Serial EEPROM

The serial EEPROM is a Microchip 24LC256 32KB type. You can use it in any way you need to; the chip is not programmed during manufacturing. Possible uses include calibration data or board ID information.

Information on communicating with the EEPROM is available from Microchip Technology, Inc.

Schematic and Layout

This appendix contains the complete bill of materials, schematic diagram, and PCB layout for the ADS1244/45EVM.

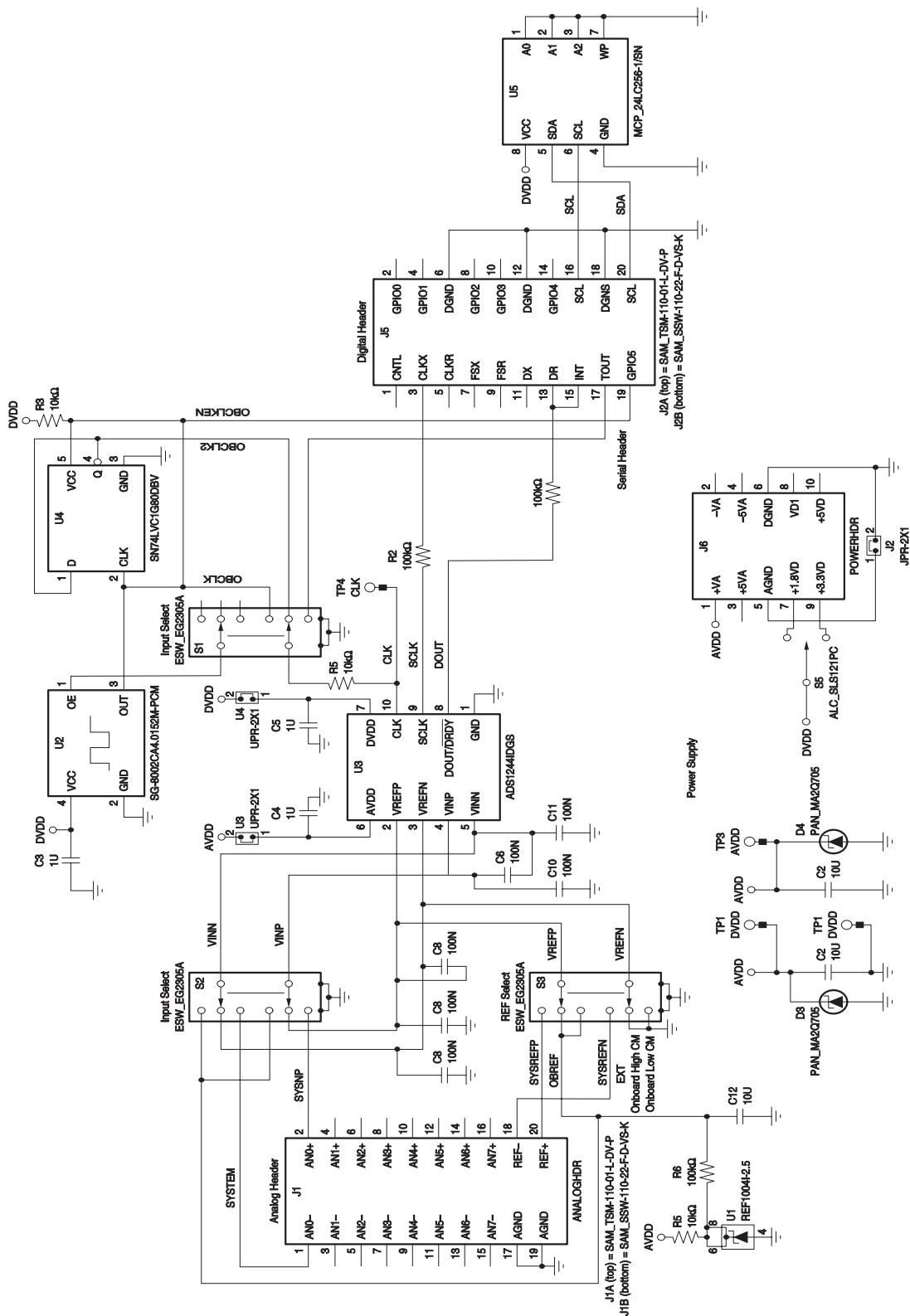
The schematic diagram is shown in Section 4.1 on page 4-2. The top (component) side layout is shown in Figure 4–2 on page 4-3. The bottom (solder) side layout is shown in Figure 4–3 on page 4-3. The bill of materials is shown in Section 4.3 on page 4-4.

Both the schematic and the bill of materials apply for the ADS1244EVM and the ADS1245EVM. The only difference between them is the part at U3. On the ADS1244EVM, U3 is ADS1244IDBG; on the ADS1245EVM, U3 is ADS1245IDBG.

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4.1 Schematic

Figure 4–1. Schematic Diagram



4.2 Board Layout

Figure 4-2. Top Side Layout

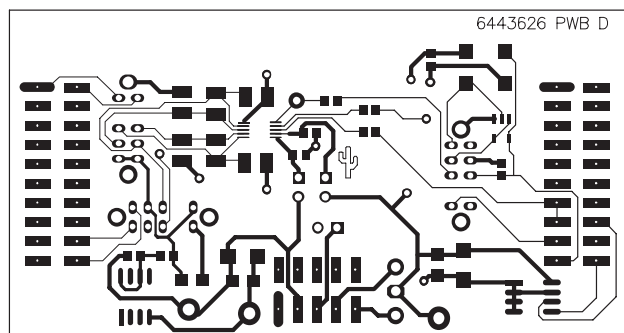
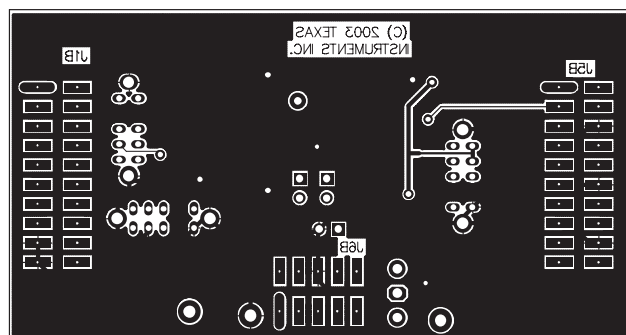


Figure 4-3. Bottom Side Layout



4.3 Bill of Materials

Table 4–1. Bill of Materials

Ref Des	Description	Vendor	Part Number
R4, R1, R6, R2	1/16W 1% 100–R Chip Resistor	Panasonic	ERJ–3GEYJ101V
R3, R5	1/16W 1% 10k Chip Resistor	Panasonic	ERJ–3GEYJ103V
C3, C4, C5	50V 1uF Ceramic Capacitor, +/- 0.5pF, NPO	Panasonic	ECJ–1VB1C105K
C1, C2, C12	16V 10 uF Ceramic Capacitor, +80% –20%, F	Panasonic	ECJ–3YF1C106Z
C8, C6, C10, C11	50V 0.1uF Ceramic Capacitor, +/- 10%, X7R	Kemet	C1210C104K5RACTU
C7, C9	Not installed		
U3	Analog–to–digital converter	Texas Instruments	ADS1244IDGS / ADS1245IDGS
U2	Oscillator	Epson	SG–8002CA4.9152M–PCM
U5	Serial EEPROM	Microchip	24LC256–I/SN
U1	Voltage reference	Texas Instruments	REF1004I–2.5
U4	Positive edge–triggered D–type flip–flop	Texas Instruments	SN74LVC1G80DBVR
D3, D4	Schottky diode	Panasonic	MA2Q705
N/A	ADS1244 EVM PWB	Texas Instruments	6443626
TP4	Test point, miniature, white	Keystone Electronics	5002
TP3	Test point, multipurpose, red	Keystone Electronics	5010
TP1	Test point, multipurpose, orange	Keystone Electronics	5013
TP2	Test point, multipurpose, black	Keystone Electronics	5011
J1A, J5A	Header, SMT, 20 pin	Samtec	TSM–110–01–T–DV–P
J1B, J5B	Socket, SMT, 20 pin	Samtec	SSW–110–22–F–D–VS–K
J6A	Header, SMT, 10 pin	Samtec	TSM–105–01–T–DV–P
J6B	Socket, SMT, 10 pin	Samtec	SSW–105–22–F–D–VS–K
J2, J3, J4	2 Position Jumper , 0.1" spacing	Samtec	TSW–102–07–L–S
S5	SPDT slide switch	Alcoswitch	SLS121PC
S1, S2, S3	DP3T slide switch	E–Switch	EG2305A